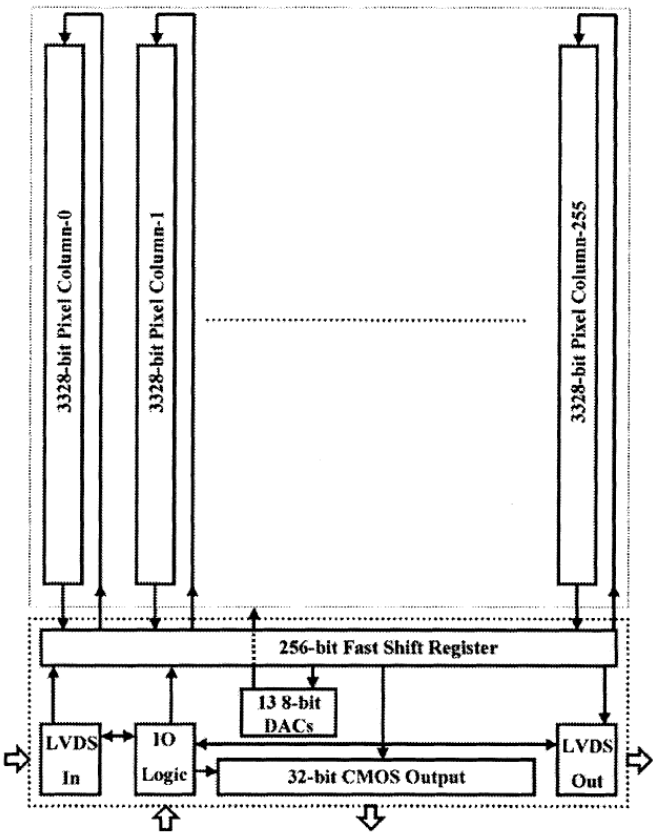
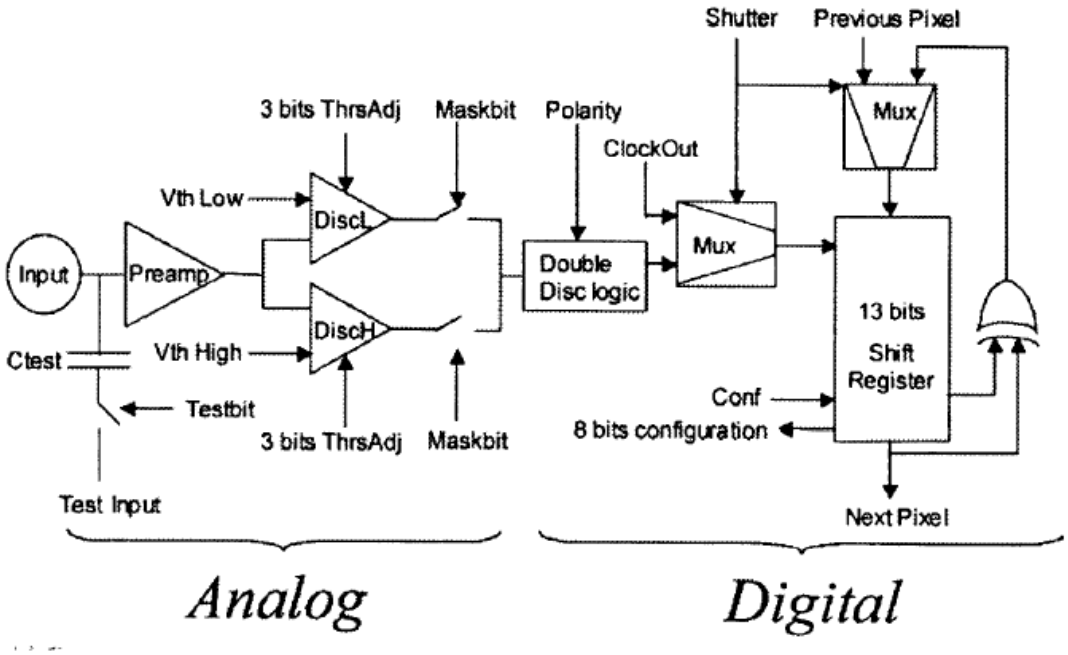
SCHEMATIC FLOOR PLAN



SCHEMATIC OF A PIXEL CELL



TECHNICAL SPECIFICATIONS

General	
Parameter	**Value**
CMOS technology	0.25 um
Pixel matrix	256 x 256
Pixel size	55 um x 55 um
Design	CERN
Features	• Energy windowing (Upper and lower threshold adjustable per pixel with 3 bits) • Single particle counting • Hit rate 100 KHz • 3-side buttable
Power supply	Two independent 2.2V power supplies for the analog and digital part
Number of transistors	~34 million
Analog front end (pixel cell)	
Parameter	**Value**
Baseline shift preamplifier output	162 e- rms
Signal polarity	Positive and negative
Detector capacitance	
Leakage current	-10 to 20 nA
Time to peak	150 ns
Noise	80 e-
Analog static power consumption	8 uW
Analog power consumption	500mW
Digital part (pixel cell + periphery)	
1 counter/shift register	14 bits (8001 counts)
periphery	• 13 8-bit DACs to set voltages in the chip • 1 256-bit Fast Shift Register to write in or readout the sensitive area • 127 I/O pads • LVDS drivers and receivers (configuration of the chip in serial mode) • Parallel 32-bit CMOS bus (chip readout can be serial or parallel)
Readout time in serial mode (100 MHz clock)	9 ms (102 Mbps)
Readout time in parallel mode (100 MHz clock)	266 us (3.5 Gbps)