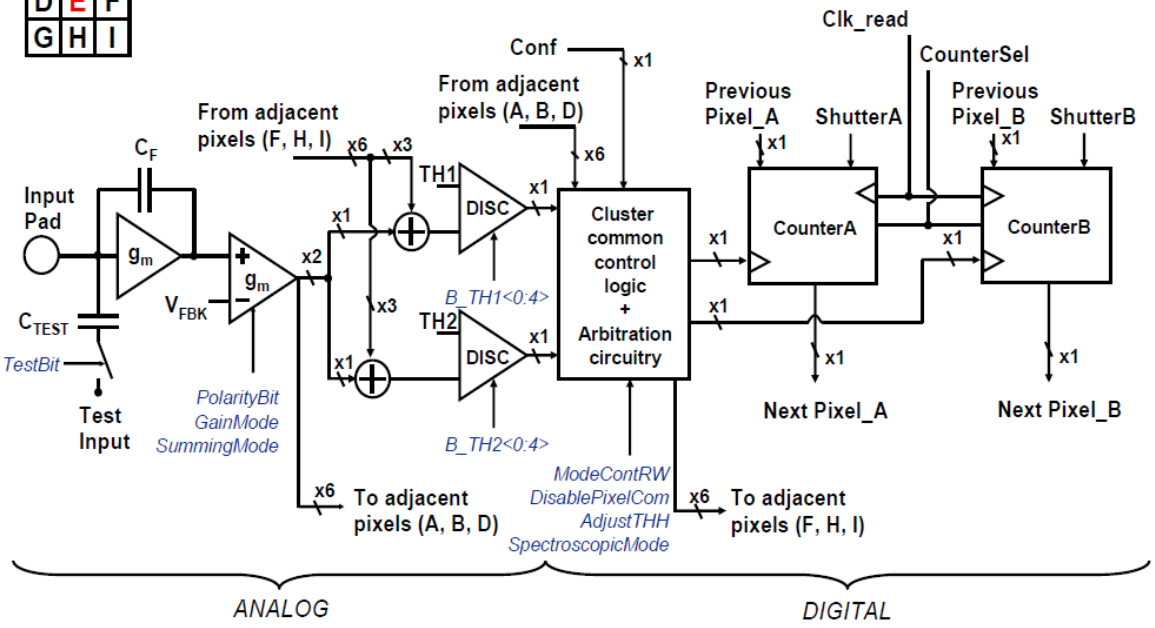
A	B	C
D	**E**	F
G	H	I

BLOCK DIAGRAM OF PIXEL E



TECHNICAL SPECIFICATIONS

General	
Parameter	**Value**
CMOS technology	0.13 um
Pixel matrix	256 x 256
Pixel size	55 um x 55 um
Design	CERN
Features	• sensor pixel can be same or four times the size of readout pixel (fine pitch and spectroscopic modes respectively) • Region of interest readout possible selecting either 32, 64 or 128 column blocks and or a number of rows to be readout • Chip IO connected through WB or TSV (dicing) to minimize dead area • Charge summing architecture • High gain mode (HG, lower linearity, lower noise) or low gain mode (LG) • Configurable counters 1, 4, 12, 24-bit • Data acquisition and readout sequential or continuous (dead time free) • 2 thresholds (adjustable independently per pixel with 5 bits) • Hit rate 100 KHz? • 4-side buttable (after dicing)
Power supply	4 power supply domains: (1) analog core 1.5V (2) digital core 1.5V (3) digital IO 2.5V (4) analog IO 3.3V (last one only for e-fuse programming)
Number of transistors	~115 million
Analog front end (pixel cell)	
Parameter	**Value**
Baseline shift preamplifier output	
Signal polarity	Positive and negative
Detector capacitance	
Leakage current	
Time to peak	110 ns
Noise	85 e- (SPM);180(CSM)
Analog static power comsumption	15 uW (CSM); 9 uW (SPM)
Analog power comsumption	600mW (SPM); 900mW (CSM)
Digital part (pixel cell + periphery)	
2 counters/shift registers	12 bits (11810 counts)
periphery	• 25 DACs (10 9-bit and 15 8-bit) to set voltages in the chip • power pads • LVDS drivers and receivers(configuration of the chip in serial mode) • Parallel data port configurable to 1, 2, 4 or 8 LVDS lines

Readout time 8 parallel LVDS lines (200 MHz clock)	500 us (1.6 Gbps)
Digital power consumption (200 MHz)	250mW