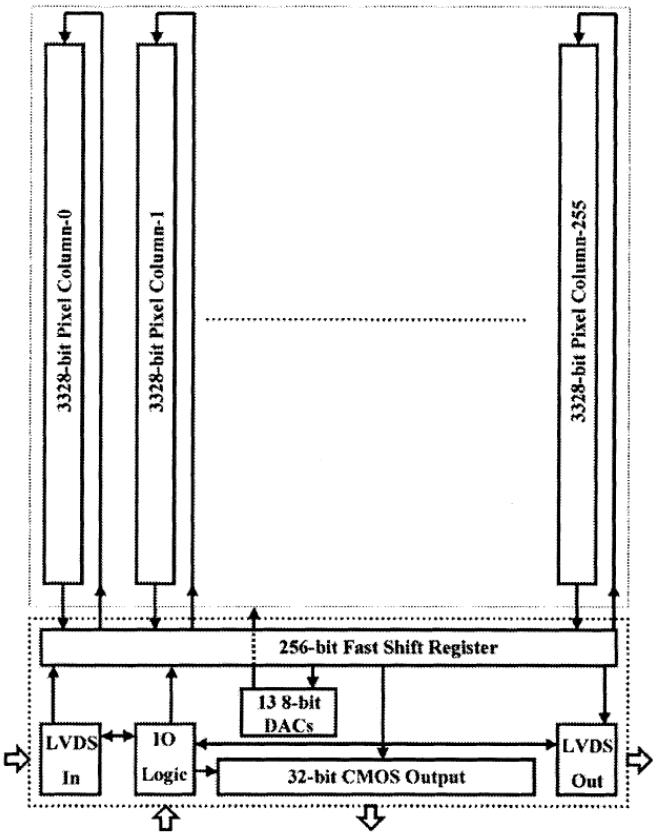
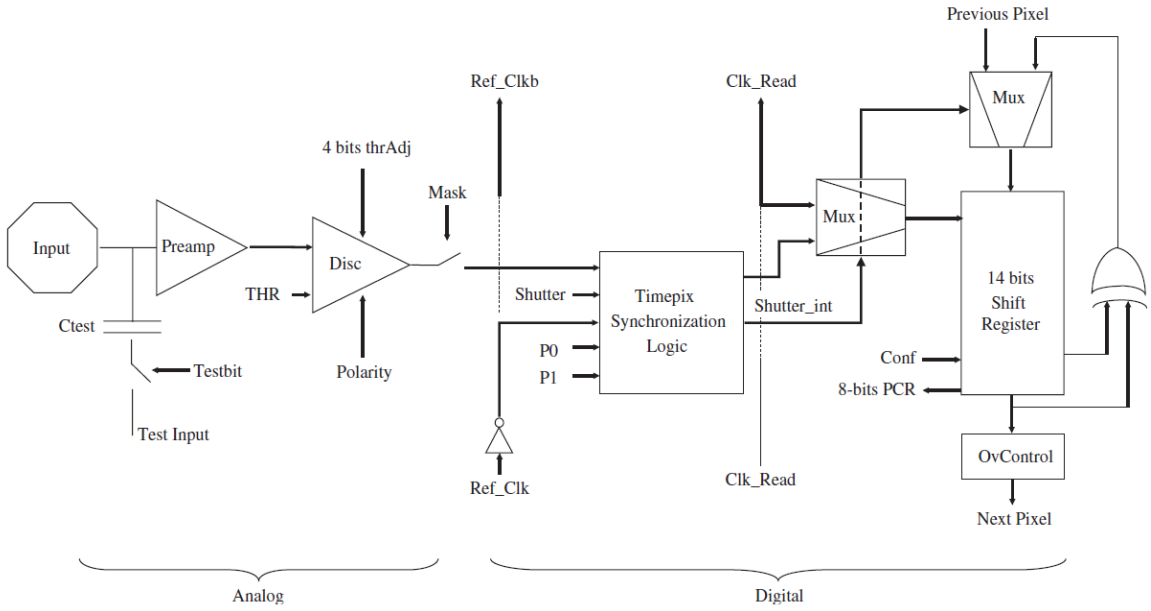
SCHEMATIC FLOOR PLAN



SCHEMATIC OF A PIXEL CELL



TECHNICAL SPECIFICATIONS

General	
Parameter	**Value**
CMOS technology	0.25 um
Pixel matrix	256 x 256
Pixel size	55 um x 55 um
Design	CERN
Features	• Single energy threshold (adjustable per pixel with 4 bits) • Three modes of operation: (1) single particle counting (2) Time over Threshold (TOT) and (3) Time of Arrival (TOA) • Can be combined with Gas Gain Grid to readout electron deposition in a gas detector • Hit rate 100 KHz • 3-side buttable
Power supply	Two independent 2.2V power supplies for the analog and digital part
Number of transistors	~36 million
Analog front end (pixel cell)	
Parameter	**Value**
Baseline shift preamplifier output	112 e- rms
Signal polarity	Positive and negative
Detector capacitance	
Leakage current	-10 to 20 nA
TOT monotonicity	Up to 200Ke-
Time to peak	110 ns
Noise	75 e-
Analog static power comsumption	6 uW
Analog power comsumption	440mW
Digital part (pixel cell + periphery)	
1 counter/shift register	14 bits (11810 counts)
periphery	• 13 8-bit DACs to set voltages in the chip • 1 256-bit Fast Shift Register to write in or readout the sensitive area • 127 I/O pads • LVDS drivers and receivers (configuration of the chip in serial mode) • Parallel 32-bit CMOS bus (chip readout can be serial or parallel)
Readout time in serial mode (100 MHz clock)	9 ms (102 Mbps)
Readout time in parallel mode (100 MHz clock)	266 us (3.5 Gbps)
Digital power comsumption	450mW